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Key

IEEE JNL	IEEE Journal or Magazine
IET JNL	IET Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IET CNF	IET Conference Proceeding
IEEE STD	IEEE Standard

1. **A Novel Ternary Controller Unit**
   Haidar, A.M.; Al-Rifai, F.; Alaeldine, A.; Bernard, M.F.;
   Information and Communication Technologies: From Theory to Applications, 2008. ICTTA 2008. 3rd International Conference on
   7-11 April 2008 Page(s):1 - 6
   Digital Object Identifier 10.1109/ICTTA.2008.4530260
   Summary: The aim of this paper is to present a new design for a controller unit using base 3, which will be named ternary controller unit. The ternary controller unit is planned to be the future brain of the ternary central processing unit. The ternary contro.....
   AbstractPlus | Full Text: PDF(239 KB) IEEE CNF
   Rights and Permissions

2. **Design and implementation of ternary exoatmospheric autopilot system**
   Choi, L.-J.; Bailey, J.M.;
   Digital Avionics Systems Conference, 1990. Proceedings., IEEE/AIAA/NASA 9th
   15-18 Oct. 1990 Page(s):58 - 63
   Digital Object Identifier 10.1109/DASC.1990.111262
   Summary: A ternary-microprocessor-based exoatmospheric autopilot system including a ternary valve servo system is designed in which the ternary processor and ternary hardware cover all navigational calculations and preprogrammed missions. The exoatmospheric a.....
   AbstractPlus | Full Text: PDF(312 KB) IEEE CNF
   Rights and Permissions

3. **A study of ternary fuzzy processor using neural networks**
   Sakamoto, M.; Morisue, M.;
   Circuits and Systems, 1997. ISCAS '97., Proceedings of 1997 IEEE International Symposium on
   Volume 1, 9-12 June 1997 Page(s):613 - 616 vol.1
   Digital Object Identifier 10.1109/ISCAS.1997.608880
   Summary: A novel ternary fuzzy processor using logic oriented neural networks is proposed, and the simulation results are illustrated to show how a ternary fuzzy inference engine can be realized by taking into consideration the advantages of neural networks. .....
   AbstractPlus | Full Text: PDF(296 KB) IEEE CNF
   Rights and Permissions

4. **A superconducting ternary systolic array processor**
Morisue, M.; Fu-Qiang Li;
Multiple-Valued Logic, 1992. Proceedings., Twenty-Second International Symposium on
27-29 May 1992 Page(s):10 - 17
Digital Object Identifier 10.1109/ISMVL.1992.186772
Summary: A novel Josephson ternary systolic array processor for multiplication is proposed. The processor consists of two kinds of cells, one of which performs a partial multiplication and the other two functions of multiplication and addition simultaneously.....
AbstractPlus | Full Text: PDF(396 KB) IEEE CNF
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5. **A high-speed interconnect network using ternary logic**
Madsen, J.K.; Long, S.I.;
Multiple-Valued Logic, 1995. Proceedings., 25th International Symposium on
23-25 May 1995 Page(s):2 - 7
Digital Object Identifier 10.1109/ISMVL.1995.513502
Summary: This paper describes the design and implementation of a high-speed interconnect network (ICN) for a multiprocessor system using ternary logic. By using ternary logic and a fast point-to-point communication technique called STARI (Self-Timed At Receiv.....
AbstractPlus | Full Text: PDF(464 KB) IEEE CNF
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6. **A Low-Power Protocol Processor Based on NAND-Type TCAMs for Networked Sensors**
Xin Xiaoning; Yu Haibin; Cui Shuping;
Wireless Communications, Networking and Mobile Computing, 2007. WiCom 2007. International Conference on
21-25 Sept. 2007 Page(s):2572 - 2575
Digital Object Identifier 10.1109/WICOM.2007.640
Summary: A Protocol Processing Accelerator based on low- power NAND-type Ternary Content Addressable Memories (TCAMs) is present in this paper. The fundamental constraint of a network sensor is the energy consumption, the high requirement on clock frequency o.....
AbstractPlus | Full Text: PDF(151 KB) IEEE CNF
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7. **Towards a Ternary Sigma-Delta Modulated Processor: Adder and Integrator**
Sadik, A.Z.; O'Shea, P.J.;
Computer and Information Technology Workshops, 2008. CIT Workshops 2008. IEEE 8th International Conference on
8-11 July 2008 Page(s):515 - 520
Digital Object Identifier 10.1109/CIT.2008.Workshops.16
Summary: Sigma delta modulated systems have a number of very appealing properties, and are therefore heavily used in analog to digital converters, amplifiers and as modulators in communication systems. This paper presents new results which show that they may .....
AbstractPlus | Full Text: PDF(293 KB) IEEE CNF
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8. **Technique to eliminate sorting in IP packet forwarding devices**
Baldwin, R.W.; Ng, E.;
Computer Design: VLSI in Computers and Processors, 2004. ICCD 2004. Proceedings. IEEE International Conference on
11-13 Oct. 2004 Page(s):554 - 559
Digital Object Identifier 10.1109/ICCD.2004.1347977
Summary: This paper presents a solution to eliminate the requirements of sorting by prefix length in IP forwarding devices using ternary content addressable memories (TCAMs). These do away with delays arising from inserting into a sorted list. To achieve this.....
AbstractPlus | Full Text: PDF(551 KB) IEEE CNF
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9. **Fast skew number computation using a CAM and related hardware for an n-bit context predictor**
Betzos, G.A.; Oldfield, J.V.;
Electronics Letters
Volume 29, Issue 14, 8 July 1993 Page(s):1265 - 1267
Digital Object Identifier 10.1049/el:19930845
Summary: An efficient way of calculating skew numbers for a binary arithmetic coder using a content-addressable memory (CAM) with ternary storage capabilities is presented. A predictor unit consisting of the CAM, context counters, MPS flags, a history buffer .....
AbstractPlus | Full Text: PDF(299 KB) IET JNL

10. **On the diagnosability of systems with three valued test results: diagnosis by comparison strategy**
Sengupta, A.; Rhee, C.;
Multiple-Valued Logic, 1990., Proceedings of the Twentieth International Symposium on
23-25 May 1990 Page(s):115 - 120
Digital Object Identifier 10.1109/ISMVL.1990.122606
Summary: A model of self-diagnosable multiprocessor systems, in which the faulty processors are determined by comparing the results of identical tasks performed by a pair of processors in the system, was introduced by J. Maeng and M. Malek (1981). An analysis.....
AbstractPlus | Full Text: PDF(440 KB) IEEE CNF
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11. **A New Moduli Set $\{3^n - 1, 3^n+1, 3^n + 2, 3^n - 2\}$ in Residue Number System**
Hosseinzadeh, M.; Jassbi, S.J.; Navi, K.;
Advanced Communication Technology, 2008. ICACT 2008. 10th International Conference on
Volume 3, 17-20 Feb. 2008 Page(s):1601 - 1603
Digital Object Identifier 10.1109/ICACT.2008.4494087
Summary: Residue Number System (RNS) is non weighted system. This system is a useful tool for Digital Signal Processing (DSP) since it can support parallel, carry-free, high-speed, low power and secure arithmetic. One of the most important considerations when.....
AbstractPlus | Full Text: PDF(672 KB) IEEE CNF
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12. **Incorporating timing constraints in the efficient memory model for symbolic ternary simulation**
Velev, M.N.; Bryant, R.E.;
Computer Design: VLSI in Computers and Processors, 1998. ICCD '98. Proceedings., International Conference on
5-7 Oct. 1998 Page(s):400 - 406
Digital Object Identifier 10.1109/ICCD.1998.727081
Summary: This paper introduces the four timing constraints of setup time, hold time, minimum delay, and maximum delay in the efficient memory model (EMM). The EMM is a behavioral model, where the number of symbolic variables used to characterize the initial s.....
AbstractPlus | Full Text: PDF(48 KB) IEEE CNF
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13. **Mixed level test generation for MOS circuits**
Lioy, A.;
European Test Conference, 1989., Proceedings of the 1st
12-14 April 1989 Page(s):208 - 211
Digital Object Identifier 10.1109/ETC.1989.36245
Summary: The authors present a test-generation system for combinational circuits described at mixed gate and switch levels. The circuit under test is hierarchically partitioned into blocks characterized by their I/O function. Only the faulty block is eventual.....
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